IN THE UNITED STATES PATENT AND TRADEMARK OFFICE PATENT APPLICATION

Appl. No.

TBD

Confirmation No. TBD

Applicant

Yunus et al.

Filed: TC/A.U. Herewith

Examiner

TBD TBD

Docket No.

TI-33423A

Customer No.

23494

Mail Stop Patent Application Commissioner for Patents P. O. Box 1450 Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97 & 1.98

Sir:

Applicant wishes to bring to the attention of the Patent and Trademark Office the information noted on the enclosed PTO Form 1449. Pursuant to the new rules, only the non-patent documents are enclosed with this statement.

Please charge any fees due in connection with the filing of this paper to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. Please credit any excess fees to the same deposit account.

Texas Instruments Incorporated P. O. Box 655474 MS 3999 Dallas, Texas 75265 (972) 917-5355 Respectfully submitted,

Attorney for Applicant(s)

Reg. No. 52,305

FORM PTO-1449 (REV. 7-80)	U.S. DEPARTMENT		CE	ATTY. DOCKET NO.			SERIAL NO.		
(REV. 7-80) PATENT AND TRADEMARK OFFICE				TI-33423A			The state of the s		
LIST OF	DOCUMENTS CITE (Use several sheets if nece		ICANT					TBD	
	APPLICANT	APPLICANT: Yunus et al.							
				FILING DATE			GRO	GROUP	
					Herewith			TBD	
		U.S. PATI	ENT DOCU	IMENTS					
*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAI	МЕ	CLASS	SUBCLASS		FILING DATE (IF APPROPRIATE)	
	US 6,213,347 B1	04/10/01	Thomas		222	52		04/30/1999	
<u> </u>	US 6,228,680 B1	05/08/01	Thomas		438	108		05/01/1999	
	US 6,245,583 B1 5,801,446	06/12/01	Amador et al.		438	778		04/30/1999	
	3,001,440	09/01/98	DiStefano e	et ai.	257	//8		03/28/1995	
			 		<u> </u>	 		,	
<u> </u>		FOREIGN PA	ATENT DC	CIMENT	2,	I			
	TOREIGNIZATE			COMILITA				TRANSLATION	
0	DOCUMENT	DATE		JNTRY		4.00			
	NUMBER	DATE		JNIKY	CLA	155	SU B		
							CL		
							AS S		
								YES NO	
<u> </u>	CONTRACTOR A COLUMN								
	OTHER NON-PATE								
"A Silicon and Aluminum Dynamic Memory Technology" Larsen, IBM J. Res. Develop. Vol 24. No. 3, May 1980, pp. 258-282									
	"Calculated Thermally Induced Stresses In Adhesively Bonded and Soldered Assemblies" Suhir,								
	AT&T Bell Laboratories, Murray Hill, New Jersey 07974, pp. 383-392								
"Clasp Ceramic Column Grid Array Technology for Flip Chip Carriers", Ray et al., Advanced									
	Packaging Technologies Tutorial, SEMICON West 99, pp. A-1 - A-7								
"Controlled Collapse Reflow Chip Joining", Miller, IBM Components Division, May 1969, pp. 239-250									
	"Die Attachment Design and Its Influence on Thermal Stresses, Suhir, AT&T Bell Laboratories, Murray Hill, New Jersey 07974, pp. 508-517								
	"Geometric Optimization of Controlled Collapse Interconnections", Goldmann, IBM Components Division, Fishkill, New York, May, 1969, pp. 251-265								
	"Reliability of Controlled Collapse Interconnections", Norris et al., IBM Components Division, May, 1969, pp. 266-271								
"SLT Device Metallurgy and Its Monolithic Extension", Totta et al., IBM J. Res. Develop. May 19								evelop. May 1969,	
pp. 226-238. "Studies of the SLT Chip Terminal Metallurgy", Berry et al., IBM J. Res. Develop., May 1969, pp. 296-206									
	286-296 "The Quality of Die-Attachment and Its Relationship to Stresses and Vertical Die-Cracking", van								
	Kessel, et al.,, 1983 IEEE, pp. 237-244 "Parametric Study of Temperature Profiles in Chips Joined by Controlled Collapse Techniques", Oktay, IBM Components Division, May 1969, pp. 272-285								
	Techniques", Oktay,	, IBM Compo	nents Divisio	n , May 196	i9, pp. 272-	-285			
EXAMINER				DATE CONS	SIDERED				
*FYAMINER: Initial if r	reference considered, whether or not ci	itation is in conforman	and with MPEP 600:	Denue line through	- situation if not	:	nd n		
of this form with next com	munication to applicant.	EXION IS IN COMOTHER	ce with MFE1 002,	Draw line unough	1 Citation is not	in contornais	се апа н	ot considered. Include copy	